In the Claims:

In the specification, please replace paragraph [0021] with the following rewritten paragraph.

-- Figure 2 illustrates another embodiment of the HEMT 10. In this embodiment, the GaN termination layer 16 further serves as a reproducible termination layer for the passivated HEMT 10. By being reproducible, the GaN termination layer 16 may be consistently reproduced each time the HEMT 10 is fabricated. In this embodiment, the HEMT 10 includes a passivation layer 32 deposited on the GaN termination layer 16. In general, the passivation layer 32 is a dielectric material that passivates, or fills, surface traps on the surface of the GaN termination layer 16, where surface traps are unfilled bonding sites in the crystalline structure due to abrupt termination of the GaN termination layer 16. The passivation layer 32 is deposited on the GaN termination layer 16 before forming the contacts 26, 28, and 30. Regions of the passivation layer 32 are etched, and the contacts 26, 28, and 30 are formed in the etched regions such that the passivation layer 32 remains between the source contact 26 and the gate contact 28 and between the gate contact 28 and the drain contact 30. One example of a passivated HEMT is disclosed in commonly owned and assigned U.S. Patent Application No. [_____] 10/689,980 entitled SURFACE PASSIVATION OF GaN DEVICES IN EPITAXIAL GROWTH CHAMBER filed on [_____] October 20, 2003, which is incorporated herein by reference in its entirety. --

In the Claims:

1. (Currently Amended) A high voltage gallium nitride (GaN) transistor structure comprising:

a) a substrate;

b) a plurality of epitaxial layers deposited on the substrate and comprising:

i) a transitional layer deposited above the substrate;

ii) a sub-buffer layer deposited above the transitional layer and adapted to increase a source-drain breakdown voltage of the GaN transistor structure by preventing ~~prevent~~ electrons from entering the transitional layer and the substrate during high voltage operation; and

iii) a GaN buffer layer deposited above the sub-buffer layer; and

c) electrical contacts deposited on the plurality of epitaxial layers, thereby forming a high electron mobility transistor.

2. (Original) The structure of claim 1 wherein the sub-buffer layer is essentially aluminum nitride.

3. (Original) The structure of claim 1 wherein the plurality of epitaxial layers further comprise a Schottky layer deposited above the GaN buffer layer.

4. (Original) The structure of claim 3 wherein the Schottky layer is essentially aluminum gallium nitride.

5. (Original) The structure of claim 3 wherein the plurality of epitaxial layers further comprise a GaN termination layer deposited above the Schottky layer and adapted to protect the Schottky layer from surface reactions.

6. (Original) The structure of claim 5 wherein the GaN termination layer is further a reproducible termination layer, thereby increasing effectiveness of passivation.

7. (Original) The structure of claim 5 wherein the GaN termination layer is sufficiently thin to allow electrons to tunnel through the GaN termination layer.

8. (Original) The structure of claim 7 wherein the GaN termination is approximately 1-2 nanometers (nm) thick.

9. (Original) The structure of claim 1 wherein the contacts comprise a source contact, a gate contact, and a drain contact, further wherein the source, gate, and drain contacts are metallic.

10. (Currently Amended) The structure of claim 9 wherein a the source-drain breakdown voltage is at least one-hundred (100) volts.

11. (Original) The structure of claim 1 wherein the transitional layer is deposited on the substrate, the sub-buffer layer is deposited on the transitional layer, and the GaN buffer layer is deposited on the sub-buffer layer.

12. (Original) The structure of claim 11 wherein the plurality of epitaxial layers further comprise:

an aluminum nitride Schottky layer deposited on the gallium nitride buffer layer; and

a GaN termination layer deposited on the Schottky layer.

13. (Currently Amended) A gallium nitride (GaN) transistor structure comprising:

a) a substrate;

b) a plurality of structural epitaxial layers deposited on the substrate and including a GaN buffer layer;

c) a GaN termination layer deposited on the plurality of structural epitaxial layers and adapted to protect the plurality of structural epitaxial layers from surface reactions, wherein the GaN termination layer is sufficiently thin to allow electrons to tunnel through the GaN termination layer and is approximately 1-2 nanometers (nm) thick; and

d) electrical contacts deposited on the GaN termination layer, thereby forming a high electron mobility transistor.

14. (Original) The structure of claim 13 wherein the GaN termination layer is further a reproducible termination layer, thereby increasing effectiveness of passivation.

15-16. (Cancelled)

17. (Original) The structure of claim 13 wherein the plurality of structural epitaxial layers further comprise a transitional layer deposited above the substrate.

18. (Original) The structure of claim 17 wherein the GaN buffer layer is deposited above the transitional layer.

19. (Original) The structure of claim 18 wherein the plurality of structural epitaxial layers further comprise a Schottky layer deposited above the GaN buffer layer.

20. (Original) The structure of claim 19 wherein the Schottky layer is essentially aluminum gallium nitride.

21. (Original) The structure of claim 13 wherein the electrical contacts comprise a source contact, a gate contact, and a drain contact, further wherein the source, gate, and drain contacts are metallic.

22-25. (Cancelled)